CMOS ACTIVE PIXEL IMAGE SENSOR

Sunetra Mendis* and Eric R. Fossum

Jet Propulsion Laboratory, California institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109

ABSTRACT

A ncw CMOS active pixel image sensor is reported. The sensor uses a 2.0 μm double-poly, double-metal foundry CMOS process and is realized as a 28 x 28 array of 40 μm x 40 μm pixels, The sensor features TTL compatible voltages, low noise and large dynamic range, and will be useful in machine vision and smart sensor applications.

* S. Mendis is a graduate student in the Dept. of Electrical Engineering, Columbia Univers

1. INTROI)1JC'J'1ON

Charge-coupled devices (CCDs) arc typically employed for image acquisition. While offering high performance, CCDs arc difficult to integrate with CMOS, complicating the integration of on-chip drive and signal processing electronics. Some achievement in on-chip signal processing with CCDs has been reported[1,2,3,4,5,6] but a fully CMOS-compatible sensor technology enabling a higher level of integration would greatly benefit many applications. Simple p-n junction photodiode arrays have been fabricated using CMOS processes but typically have high read noise and suffer from image lag[7]. Both bipolar[8] and charge modulation device[9] image sensors are compatible with CMOS integration, but require specialized fabrication processes. In this paper, a new, 100°/0 CMOS-compatible image sensor with good performance is reported.

II. ACTIVE PIXEL SENSOR DESIGN AND OPERATION

The CMOS active pixel sensor is shown schematically in Fig. 1. For discussing the operation of' the image sensor, it is assumed that the sensor is operated with voltage rails of O and + 5 volts, though higher and lower voltage operation is possible and has been demonstrated. Operation of the sensor is as follows. During signal integration, the pixel photogate (PG) is biased at + 5 volts, the transfer gate TX is biased at + 2.5 volts, and the reset transistor R and selection transistor S arc both biased off (O volts), Following integration, all pixels in the row to be read are read out simultaneously onto column lines by the following process. First, the pixels are addressed by the row selection transistor S biased at + 5 volts. This activates the source-fo]]owcr output transistor in each pixel (the load transistor is located at the bottom of the pixel column and is biased at + 2.5 volts), The reset gate R is then briefly pulsed to + 5 volts to reset the floating diffusion output node FD to approximately + 3.5 volts. The output of the source-follower is then sampled onto a holding capacitor at the bottom of the column. The photogate PG is then pulsed low to O volts (with TX held at + 2.5 volts) to transfer the integrated signal charge under the photogate to the floating diffusion output node FD. The new source-follower output voltage is sampled onto a second holding capacitor at the bottom of the column, Storing the reset level and the signal level on separate capacitors permits correlated double sampling of the pixel[10], eliminating kTC noise from the pixel, and suppressing 1/f noise and fixed pattern noise from the output transistor. In this circuit, the major source of readout noise is the kTC noise introduced by the sample/hold capacitors, since kTC noise from the pixel is suppressed by the differential output technique. The r.m.s. noise on these 1pF capacitors is estimated to bc 64 μV per capacitor, or 91 μV in differential mode,

All transistor were sized in anticipation of a 128x1 28 array size readout at the rate of 30 Hz corresponding to a row readout time of 260 μsec/row. The total time to capture the row signal, in parallel, to the bank of capacitors at the bottom of each column was designed to be 0.7 μsec. The capacitors are sequentially scanned for serial readout,

The APS was designed using highly conservative 2 μm CMOS design rules and practices The array was sized at 28 x 28 to fit within a standard 2 mm MOSIS tiny chip

factor of the 40 μm x 40 μm pixel, as measured by the ratio of active area (by design) to the total pixel area, is 26°/0. Use of less conservative 2 μm design rules and practices could likely increase the fill-factor of the pixel to 350A.

The row and column selection 5-to-32 decoders were implemented using a standard 5-input NAND gate designed to tit in the 40 μm pixel pitch, The PG and R pulses were gated with the row selection. The reset and signal channels for each column were laid out to be as symmetric as possible to ensure good cornmon-mode rejection and differential output. The digital decoder was designed to be highly isolated from the column-wise analog circuitry. A light shield surrounding the imaging area was made using second level metal. A photograph of the completed sensor is shown in Fig. 2.

111. EXPERIMENTAL RESULTS

The image sensors were driven in accordance to the timing and voltage levels described above. A sample image is shown in Fig. 3. Using an electrical test circuit on a separate IC, output conversion was determined to be 4.0 pV/electron. Saturation was measured to be 600 mV, or 150,000 electrons. The saturation level was determined by the output amplifier rather than well capacity since the 2.5 volt well capacity was estimated to be approximately 6x1 0^6 electrons for this surface-channel device. No lag was observed. The design of the CMOS APS reset transistor results in a lateral anti-blooming drain so that blooming is suppressed, Using the measured conversion gain, r.m.s. noise was estimated to be 23 electrons yielding a dynamic range of 76 dB. The fixed pattern noise (FPN) was approximately 1.5°/0 p-p of the saturation level. It is believed that this can be reduced in future designs. Dark current was found to be well-behaved and measured to be approximately 2-3 nA/cm^2 at ambient temperature, though several non-saturating dark current spikes were observed.,

IV, CONCLUSION

The first **100%** CMOS active pixel image sensor has been demonstrated. The high performance obtained using standard foundry CMOS has encouraged us to pursue the fabrication of a 128 x 128 CMOS APS in the near future. A reduction in noise of more than a factor of 2, an increase in fill-factor to 35%, and reduction in FPN to below O.5% p-p is believed to be readily feasible in later generations. The usc of 0.8 μm design rules could yield a 15 μm x 15 μm pixel size. Coupled with a microlens technology, the effective aperture could reach 65°/0 or more, This initial work paves the way for more complex pixel structures and on-chip electronics for robot vision, guidance and navigation, and other smart sensor applications.

V. ACKNOWLEDGMENTS

The authors appreciate useful conversations and encouragement from our colleagues at JPL, especially B. Pain, C. Stevens, S. Kemeny, B. Wilcox and R. Bartman. The support of V. Sarohia of JPL and W. Hudson of NASA 1 IQ is gratefully acknowledged

The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Defense Advanced Research Projects Agency and the National Aeronautics and Space Administration.

VI. REFERENCES

[1]E.R. Fossum, "Ct~argc-coupled computing for focal-plane image processing," Optical Engineering, vol. 26(9) pp. 916-922 (1 987).

[2]E.R. Fossum, "Architectures for focal-plane image processing," Optical Engineering, vol. 28(8) pp. 865-871 (1989).

[3]W. Yang and A. Chiang, "A full-fill factor CCD imager with integrated signal processors," Pmt. 1990 IEEE International Solid-State Circuits Conference, pp. 218-219 (1990).

[4]E-S.Eid and E.R.Fossum, "Real time focal-plane array image processor, " in Automated Inspection and High Speed Vision Architectures 111, Pmt. SPIE vol. 1197, paper 1 (1989).

[5]S.E. Kemeny, E-S. Eid, S. Mendis and E.R. Fossum, "Update on focal-plane image processing research", in Charge-Coupled Devices and Solid-State Optical Sensors 11, Proc. SPIE vol. 1447, pp. 243-250 (1991).

[6]S. E. Kemeny, H. Torbey, H. Meadows, R, Bredthauer, M. LaShell, and E.R. Fossum, "CCD focal-plane image reorganization processors for lossless image compression, " IEEE 1. Solid-State Circuits, vol. 27(3) pp. 398-405 (1992).

[7]Yadid-Pecht, R. Ginosar, and Y. Shacham Diamand, "A random access photodiode array for intelligent image capture", IEEE 7'rans.Electron Devices, vol. 38(8), pp. 1772-1780 (1991).

[8]Tanaka, S. Hashimoto, M. Shinohara, S. Sugawa, M, Morishita, S. Matsumoto, Y. Nakamura, and T. Ohmi, "A 310 k-pixel bipolar imager (BASIS)," IEEE Trans. Electron Devices, vol. 37(4) pp. 964-971 (1990).

[9]M.Ogata, T. Nakamura, K. Matsumoto, R. Ohta, and R. Hyuga, "A small pixel CMD image sensor, " IEEE Trans. Electron Devices, vol. 38(S) pp. 1005-1010(1991).

[10]M. White, D. Lampe, F. Blaha, and I. Mack, "Characterization sof surface channel CCD image arrays at low light levels," IEEE J. Solid-State Circuits, vol. 9, pp. 1-13 (1974),

VII. FIGURE CAPTIONS

Fig. 1. Schematic illustration of image sensor circuit. Dotted line shows boundary of in-pixel circuits. Remainder of circuit is at bottom of column.

Fig. 2. Photograph of fabricated CMOS APS array.

Fig. 3. Photograph taken from display of28x28 image of George Washington taken from US $1 bill.

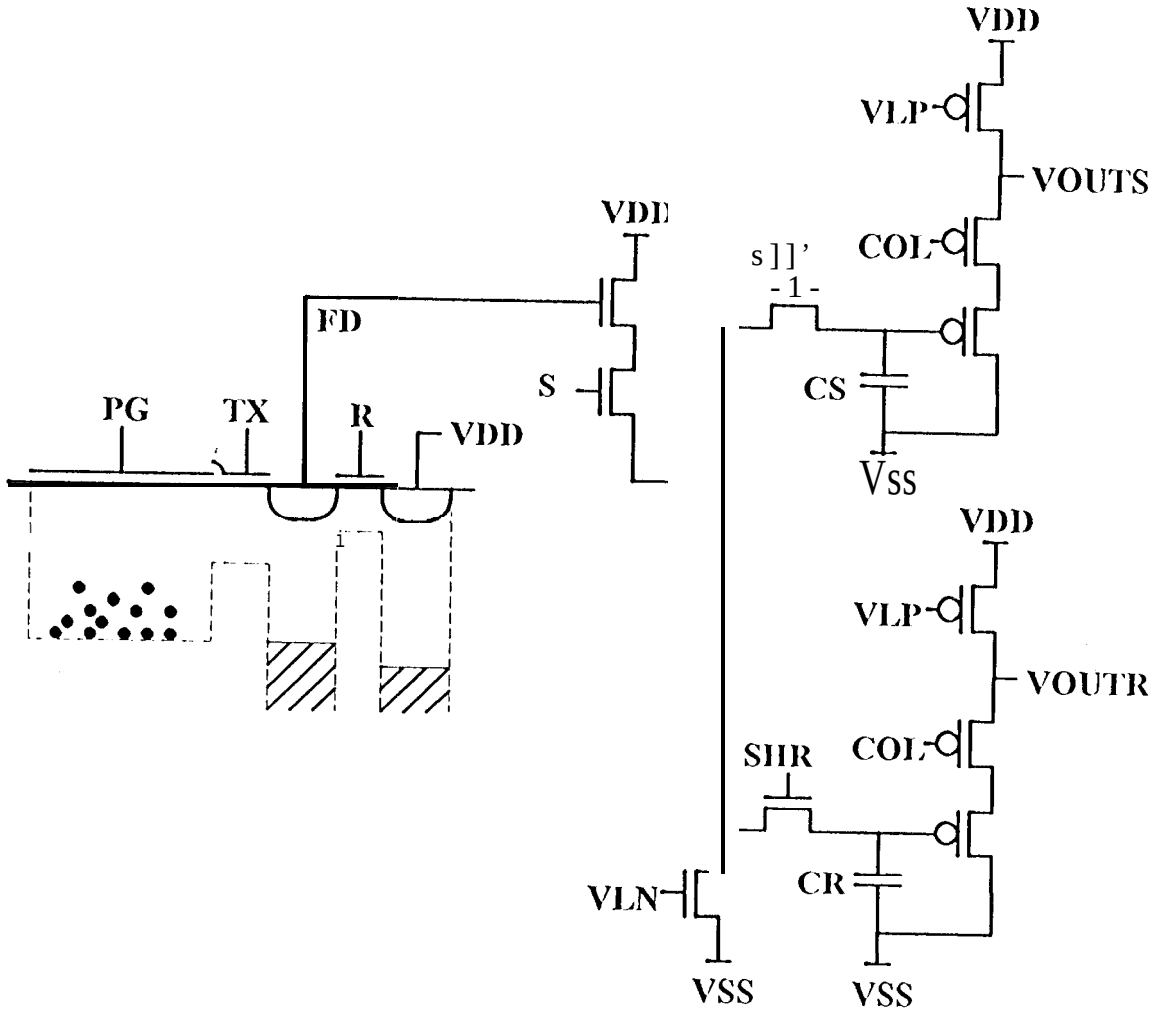

Fig. 1. Schematic illustration of image sensor circuit, Dotted line shows boundary of in-pixel circuits. Remainder of circuit is at bottom of column.

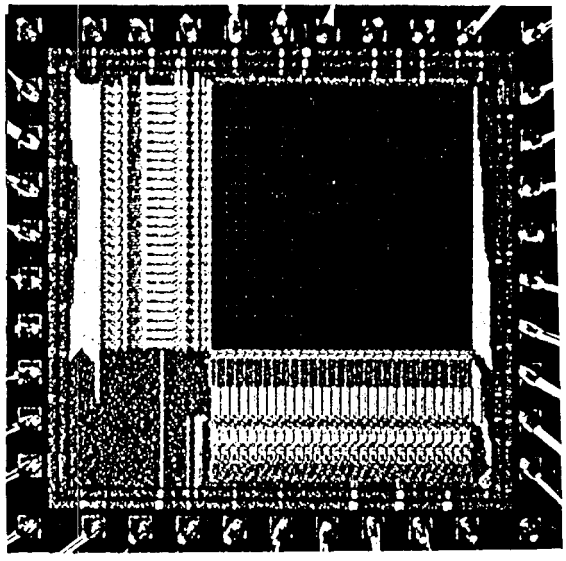

Fig. 2. Photograph of fabricated CMOS APS array.

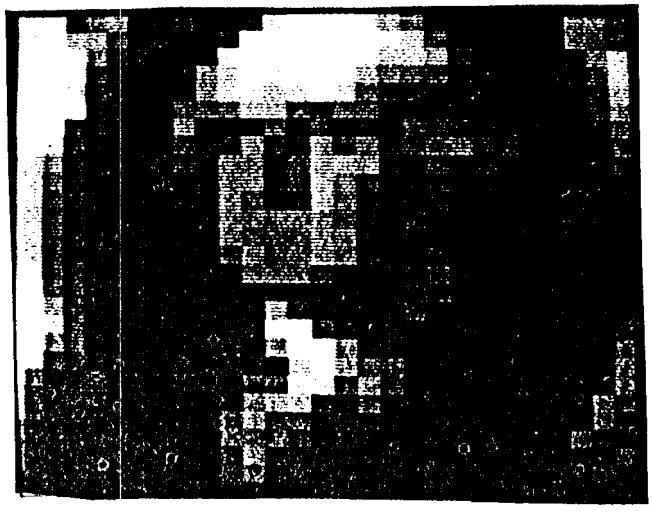

Fig. 3. Photograph taken from display of 28x28 image of George Washington t aken from US $1 bill.